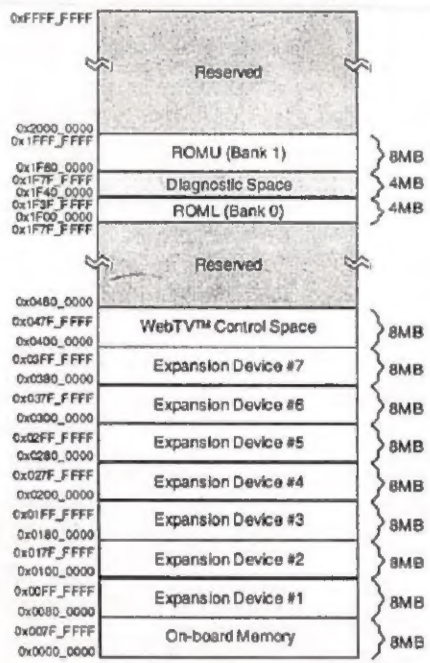
[redacted]

4. Spot Programmer's Model

4.1 Memory Map

The following figure outlines the memory map of the WebTV™ system.

Figure 4-1 WebTV™ Memory Map



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4.2 Registers

There are several registers located in the control space of SPOT (FIDO). These registers are oulined below. The 3-leter prefix before the register name indicates which unit within SPOT the register actually resides. The registers can be referred to with or without these 3-letter prefixes. NOTE: ALL REGISTERS ARE ONLY ACCESSIBLE AS ALIGNED WORDS (32-BITS).

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Table 4-1 SPOT Registers

Address	Register Name	Meaning	R/W
0x0400_0000	BUS_CHIPID	SPOT chip ID	R-only
0x0400_0004	BUS_CHPCNTL	SPOT chip control register	R/W
0x0400_0008	BUS_INTSTAT	Interrupt status register	R-only
0x0400_000C	BUS_INTEN_S	Interrupt enable register - set	R/W
0x0400_0010	BUS_ERRSTAT	Error status register	R-only
0x0400_0014	BUS_ERREN_S	Error enable register	R/W
0x0400_0018	BUS_ERRADDR	Error address register	R-only
0x0400_001C	BUS_FENADDR1	Fence lower bound 1 register	R/W
0x0400_0020	BUS_FENMASK1	Fence upper bound 1 register	R/W
0x0400_0024	BUS_ FENADDR2	Fence lower bound 2 register	R/W
0x0400_0028	BUS_ FENMASK2	Fence upper bound 2 register	R/W
0x0400_002C - 0x0400_0108	reserved	reserved for future use w/i busUnit	NA
0x0400_0108	BUS_INTSTAT_C	Interrupt status register - clear	W-only
0x0400_010C	BUS_INTEN_C	Interrupt ~~status~~ enable register - clear	W-only
0x0400_0110	BUS_ERRSTAT_C	Error status register - clear	W-only
0x0400_0114	BUS_ERREN_C	Error enable register - clear	W-only
0x0400_0118	BUS_WDREG_C	Reset watchdog register	W-only
0x0400_0120 - 0x0400_0FFF	reserved	reserved for future use	NA
0x0400_1000	ROM_SYSCONF	System Configuratrion	R-only
0x0400_1004	ROM_CNTL0	ROM control register for Bank 0	R/W
0x0400_1008	ROM_CNTL1	ROM control register for Bank 1	R/W
0x0400_1008 - 0x0400_1FFF	reserved	reserved for future use	NA
0x0400_2000	AUD_CSTART	Audio DMA current buffer start address	R–only
0x0400_2004	AUD_CSIZE	Audio DMA current buffer size	R–only
0x0400_2008	AUD_CCONFIG	Audio current channel configuration	R/W
0x0400_200C	AUD_CCNT	Audio DMA current buffer index	R–only
0x0400_2010	AUD_NSTART	Audio DMA next buffer start address	R/W
0x0400_2014	AUD_NSIZE	Audio DMA next buffer size	R/W
0x0400_2018	AUD_NCONFIG	Audio next channel configuration	R/W
0x0400_201C	AUD_DMACNTL	Audio DMA engine control	R/W
0x0400_2020 - 0x0400_2FFF	reserved	reserved for future use	NA
0x0400_3000	VID_CSTART	Video DMA current buffer start address	R–only
0x0400_3004	VID_CSIZE	Video DMA current buffer size	R–only
0x0400_3008	VID_CCNT	Video DMA current buffer index	R–only
0x0400_300C	VID_NSTART	Video DMA next buffer start address	R/W
0x0400_3010	VID_NSIZE	Video DMA next buffer size	R/W
0x0400_3014	VID_DMACNTL	Video DMA engine control	R/W

Address	Register Name	Meaning	R/W
0x0400_3018	VID_FCNTL	Video general function control	R/W
0x0400_301C	VID_BLNKCOL	Blank color register	R/W
0x0400_3020	VID_HSTART	Horizontal start of active pixels	R/W
0x0400_3024	VID_HSIZE	Horizontal size of active pixels	R/W
0x0400_3028	VID_VSTART	Vertical start of active pixels	R/W
0x0400_302c	VID_VSIZE	Vertical size of active pixels	R/W
0x0400_3030	VID_HINTLINE	Horizontal line to interrupt on	R/W
0x0400_3034	VID_CLINE	Current line the vidUnit is displaying	R-only
0x0400_3038	VID_INTSTAT	Video interrupt status	R-only
0x0400_303c	VID_INTEN_S	Video interrupt enable - set	R/W
0x0400_3040 - 0x0400_3130	reserved	reserved for future use w/i vidUnit	NA
0x0400_3138	VID_INTSTAT_C	Video interrupt status - clear	W-only
0x0400_313c	VID_INTEN_C	Video interrupt enable - clear	W-only
0x0400_3040 - 0x0400_3FFF	reserved	reserved for future use	NA
0x0400_4000	DEV_IRDATA	IR receiver data	R–only
0x0400_4004	DEV_LED	LED control register	R/W
0x0400_4008	DEV_IDCNTL	ID chip control and data reigster	R/W
0x0400_400c	DEV_NVCNTL	NVRAM control and data register	R/W
0x0400_4010	DEV_SCCNTL	SmartCard control and data register	R/W
0x0400_4014	DEV_EXTTIME	External timing control register	R/W
0x0400_4018 - 0x0400_401c	reserved	reserved for future use	NA
0x0400_4020 - 0x0400_403c	DEV_KBD0 - DEV_KBD7	Keyboard registers (8)	R/W
0x0400_4040 - 0x0400_405c	DEV_MOD0 - DEV_MOD7	Modem registers (8)	R/W
0x0400_403c - 0x0400_4FFF	reserved	reserved for future use	NA
0x0400_5000	MEM_CNTL	Memory control register	R/W
0x0400_5004	MEM_REFCNT	Memory refresh count	R/W
0x0400_5008	MEM_DATA	Memory data register	R/W
0x0400_500c	MEM_CMD	Memory command register	W-only
0x0400_5010	MEM_TIMING	Memory Timing Register	R/W
0x0400_5014 - 0x047F_FFFF	reserved	reserved for future use	NA

4.2.1 busUnit Registers

4.2.1.1 BUS_CHIPID Register

This register can be read by software to determine the ID of the SPOT chip. All WebTV ASICS will have this register defined at the same location.

Table 4-2 BUS_CHIPID Bit Definition

Bits	Symbol	Meaning
31:24	CHIPID[7:0]	Chip identification. See Appendix B for encoding..
23:20	CHIPREV[3:0]	Revision of silicon. Set to 0x0 in SPOT initially and increments on each revision.
19:16	CHIPFAB[3:0]	Manufacturer of silicon. See Appendix B for encoding. SPOT will be done with ChipExpress initially (0x0).
15:0	RESERVED	Reserved for future use.

4.2.1.2 BUS_CHPCNTL Register

This register controls variouis global chip functions such as reset watchdog timer, audio clock dividers, and time-out counts.

Table 4-3 BUS_CHPCNTL Bit Definition

Bits	Symbol	Meaning
31:30	WDENAB	Writing a special sequence to this field will enable and disable the reset watchdog timer in the busUnit. To enable the watchdog counter, software must write the following sequence: 0b00 -> 0b01 -> 0b10 -> 0b11. To disable the watchdog counter, software must write the following sequence: 0b11-> 0b10 -> 0b01 -> 0b00. After reset this field will read back as 0b00. This watchdog timer will reset the system if 64 VSYNC's have elapsed before software writes the BUS_WDREG to reset the counter.
29:26	AUDCLKDIV[3:0]	Audio clock dividor. See table below for encoding. After reset, this field is set to 0x0.
25:16	RESERVED	Reserved for future use.
15:0	TOCOUNT[15:0]	Timeout count value. This value in this field is compared against the time out counter. When the time out counter reaches this value an error ack is returned to the CPU on reads. On reset, this field is set to 0xFFFF.

Table 4-4 AUDCLKDIV Encoding

AUDCLKDIV[3:0]	Encoding
0b0000	External clock source being used
0b0001	Divide AUD_XTALI by 1 for AUD_CLK
0b0010	Divide AUD_XTALI by 2 for AUD_CLK
0b0011	Divide AUD_XTALI by 3 for AUD_CLK
0b0100	Divide AUD_XTALI by 4 for AUD_CLK
0b0101	Divide AUD_XTALI by 5 for AUD_CLK
0b0110	Divide AUD_XTALI by 6 for AUD_CLK
0b0111 - 0b1111	Reserved for future use

4.2.1.3 BUS_INTSTAT Register

This register provides most of the status of any interrupt generated from SPOT. Whenever an interrupt is detected by the enable being set and a device interrupting, SPOT will assert the CPU_INT_N signal and keep it asserted until the source of the interrupt is disabled.

Table 4-5 BUS_INTSTAT Bit Definition

Bits	Symbol	Meaning
31:8	RESERVED	Reserved for future use.
7	VIDINT	When this bit is set to '1', a vidUnit interrupt has occurred due to any of the video interrupts occuring. The real video source needs to be obtained by reading the VID_INTSTAT register in the vidUnit. Clearing the interrupt is done by writing a '1' to the corresponding bit in the BUS_INTSTAT_C register. A clear must also be done to one of the bits in the VID_INTSTAT_C register for the interrupt to be completely cleared.
6	DEVKBD	When this bit is set to '1', a devUnit interrupt has occurred due to the external keyboard controller chip asserting its interrupt line Clearing the interrupt is done by writing a '1' to the corresponding bit in the BUS_INTSTAT_C register..
5	DEVMOD	When this bit is set to '1', a devUnit interrupt has occurred due to the external modem controller chip asserting its interrupt line Clearing the interrupt is done by writing a '1' to the corresponding bit in the BUS_INTSTAT_C register..
4	DEVIR	When this bit is set to '1', a devUnit interrupt has occurred due to an IR interface data transfer being completed and ready for reading. Clearing the interrupt is done by writing a '1' to the corresponding bit in the BUS_INTSTAT_C register.
3	DEVSMC	When this bit is set to '1', a devUnit interrupt has occurred due to a SmartCard being inserted Clearing the interrupt is done by writing a '1' to the corresponding bit in the BUS_INTSTAT_C register.
2	AUDDMA	When this bit is set to '1', an audUnit interrupt has occurred due to the DMA completing. Clearing the interrupt is done by writing a '1' to the corresponding bit in the BUS_INTSTAT_C register.
1:0	RESERVED	Reserved for future use. These bit s will read back as '0'

4.2.1.4 BUS_INTEN Register

This register (register pair) is used to enable and disable the global interrupts in the chip.

Table 4-6 BUS_ INTEN Bit Definition

Bits	Symbol	Meaning
31:8	RESERVED	Reserved for future use.
7	VIDEN	When '1', this bit enables video interrupts to pass through and be seen by the CPU. When '0', video interrutps are disabled. Software must write a '1 to BUS_INTEN_S location to set the bit and write a '1' to the BUS_INTEN_C location to clear the bit. This bit is set to '0 after reset.
6	DEVKBDEN	When '1', this bit enables keyboard interrupts to pass through and be seen by the CPU. When '0', keyboard interrutps are disabled. Software must write a '1 to BUS_INTEN_S location to set the bit and write a '1' to the BUS_INTEN_C location to clear the bit. This bit is set to '0 after reset.
5	DEVMODEN	When '1', this bit enables modem interrupts to pass through and be seen by the CPU. When '0', modem interrutps are disabled. Software must write a '1 to BUS_INTEN_S location to set the bit and write a '1' to the BUS_INTEN_C location to clear the bit. This bit is set to '0 after reset.
4	DEVIREN	When '1', this bit enables IR interrupts to pass through and be seen by the CPU. When '0', IR interrutps are disabled. Software must write a '1 to BUS_INTEN_S location to set the bit and write a '1' to the BUS_INTEN_C location to clear the bit. This bit is set to '0 after reset.
3	DEVSMCEN	When '1', this bit enables SmartCard interrupts to pass through and be seen by the CPU. When '0', SmartCard interrutps are disabled. Software must write a '1 to BUS_INTEN_S location to set the bit and write a '1' to the BUS_INTEN_C location to clear the bit. This bit is set to '0 after reset.
2	AUDDMAEN	When '1', this bit enables audio DMA interrupts to pass through and be seen by the CPU. When '0', audio DMA interrutps are disabled. Software must write a '1 to BUS_INTEN_S location to set the bit and write a '1' to the BUS_INTEN_C location to clear the bit. This bit is set to '0 after reset.
1:0	RESERVED	Reserved for future use.

4.2.1.5 BUS_ERRSTAT Register

This register (register pair) is used to get the status of the most recent error which occurred in the system. Note that internal DMA transactions which are sent to a non-present expansion device will completely hang the system. It is up to software to ensure this does not happen or upon detection of a DMA transaction which has not completed after a ridiculously long time to reset the system via the watchdog timer. This sort of error will not be detected and flagged in the hardware.

Table 4-7 BUS_ERRSTAT Bit Definition

Bits	Symbol	Meaning
31:5	RESERVED	Reserved for future use.
6	F1READ	When '1', this bit indicates that the most recent error ack was due to a read fence check violation between fence register set 1 taking place in the system. After reset, this bit is '0'. After detection, this bit must be cleared by writing a '1' to the BUS_ERRSTAT_C register in order to enable another error.
5	F1WRITE	When '1', this bit indicates that the most recent error ack was due to a write fence check violation between fence register set 1 taking place in the system. After reset, this bit is '0'. After detection, this bit must be cleared by writing a '1' to the BUS_ERRSTAT_C register in order to enable another error.
4	F2READ	When '1', this bit indicates that the most recent error ack was due to a read fence check violation between fence register set 2 taking place in the system. After reset, this bit is '0'. After detection, this bit must be cleared by writing a '1' to the BUS_ERRSTAT_C register in order to enable another error.
3	F2WRITE	When '1', this bit indicates that the most recent error ack was due to a write fence check violation between fence register set 2 taking place in the system. After reset, this bit is '0'. After detection, this bit must be cleared by writing a '1' to the BUS_ERRSTAT_C register in order to enable another error.
2	TIMEOUT	When '1', this bit indicates that the most recent error ack was due to a timeout taking place in the system. Read timeouts are synchronous, write timeouts are asynchronous. The write timeouts are flagged in conjunction with the BUS_INTSTAT register. After reset, this bit is '0'. After detection, this bit must be cleared by writing a '1' to the BUS_ERRSTAT_C register in order to enable another error.
1	RESERVED	Reserved for future use.
0	OW	When '1', this bit indicates that another error occurred before the first could be serviced by the CPU.

4.2.1.6 BUS_ERREN Register

This register (register pair) is used to enable the various error-checking mechanisms in hardware.

Table 4-8 BUS_ERREN Bit Definition

Bits	Symbol	Meaning
31:5	RESERVED	Reserved for future use.
6	F1RDEN	When '1', this bit indicates read errors on fence register set 1 are enabled. After reset, this bit is '0'.
5	F1WREN	When '1', this bit indicates write errors on fence register set 1 are enabled. After reset, this bit is '0'.
4	F2RDEN	When '1', this bit indicates read errors on fence register set 1 are enabled. After reset, this bit is '0'.
3	F2WREN	When '1', this bit indicates write errors on fence register set 2 are enabled. After reset, this bit is '0'.
2	TIMEEN	When '1', this bit indicates tiem-outs on the bus are enabled. After reset, this bit is '0'.
1:0	RESERVED	Reserved for future use.

4.2.1.7 BUS_ERRADDR Register

This register is used to flag the address which encountered an error.

Table 4-9 BUS_ERRADDR Bit Definition

Bits	Symbol	Meaning
31:0	ADDR[31:0]	This field captures the most recent address which caused the error flagged in the BUS_ERRSTAT register. After reset this field is undefined.

4.2.1.8 BUS_WDREG_C Register

Software must whack this register before 64 VSYNC's elapse once the watchdog counter is enabled or else the system will hard reset.

Table 4-10 BUS_WDREG_C Bit Definition

Bits	Symbol	Meaning
31:1	RESERVED	Reserved for future use.
0	WDCLEAR	Writing a '1' to this field resets the watchdog counter. Writing a '0' has no effect. This register cannot be read.

4.2.1.9 BUS_FENADDR1 Register

This register is used to hold the address value of the lower bounds on a fence check reigster pair. Note that only main memory address space is checked.

Table 4-11 BUS_ FENADDR1 Bit Definition

Bits	Symbol	Meaning
31:24	RESERVED	Reserved for future use.
23:5	ADDR[23:5]	This field contains the address of the lower bound which the busUnit checks all main memory CPU accesses against for register set 1. After reset, this register is undefined and must be initialized prior to enabling fence checking or unpredictable results will occur.

4.2.1.10 BUS_FENMASK1 Register

This register is used to hold the mask for FENADDR1.

Table 4-12 BUS_ FENMASK1 Bit Definition

Bits	Symbol	Meaning
31:24	RESERVED	Reserved for future use.
23:5	MASK[23:5]	Fence check equation: ~|(addr[31:24], addr[23:21]^fenAddr[23:21], (addr[20:5]^fenAddr[20:5])&fenMask[23:5])

4.2.1.11 BUS_FENADDR2 Register

This register is used to hold the address value of the lower bounds on a fence check reigster pair. Note that only main memory address space is checked.

Table 4-13 BUS_ FENADDR2 Bit Definition

Bits	Symbol	Meaning
31:24	RESERVED	Reserved for future use.
23:5	ADDR[23:5]	This field contains the address of the lower bound which the busUnit checks all main memory CPU accesses against for register set 2. After reset, this register is undefined and must be initialized prior to enabling fence checking or unpredictable results will occur.

4.2.1.12 BUS_FENMASK2 Register

This register is used to hold the mask for FENADDR2.

Table 4-14 BUS_ FENMASK2 Bit Definition

Bits	Symbol	Meaning
31:24	RESERVED	Reserved for future use.
23:5	MASK[23:5]	Fence check equation: ~|(addr[31:24], addr[23:21]^fenAddr[23:21], (addr[20:5]^fenAddr[20:5])&fenMask[23:5])

4.2.2 romUnit Register

4.2.2.1 ROM_SYSCONFIG Register

This register is used to flag system configuration information to both software as well as hardware. Some of these bits are used to program the SPOT chip directly. Most are used so software can configure the hardware properly. This register is actually the ROM_DATA[31:0] bus value which is captured when reset goes away. Software is expected to figure out the system (CPU) clock frequency by using veritcal interrupts and the NTSC bit.

Table 4-15 ROM_SYSCONFIG Bit Definition

Bits	Symbol	Meaning
31	ROMTYP0	When '1', this bit means there is mask ROM present in the system for Bank 0 ROM space. If '0', then Flash ROM is present.
30	ROMMODE0	When '1', this bit means the memory devices in ROM Bank 0 support page mode. When '0', no page mode us supported.
29:28	ROMSPD0[1:0]	This field indicates the speed of the ROM present in bank 0 of ROM space. See tables below for encoding.
27	ROMTYP1	When '1', this bit means there is mask ROM present in the system for Bank 1 ROM space. If '0', then Flash ROM is present.
26	ROMMODE1	When '1', this bit means the memory devices in ROM Bank 1 support page mode. When '0', no page mode us supported.
25:24	ROMSPD1[1:0]	This field indicates the speed of the ROM present in bank 1 of ROM space. See tables below for encoding.
23:22	MEMSPD[1:0]	This field indicates the speed of the memory present in the system. See tables below for encoding.
21:20	MEMVEND[1:0]	This field indicates the particular SGRAM present in the system. Note that vendors canot be intermixed. See tables below for encoding.
19:18	AUDDACTYP[1:0]	This field indicates the type of audio DAC present in the system. See tables below for encoding.
17	AUDDACMODE	A '1' in this field indicates the clock for the audio DAC originates external to the SPOT chip. and the AUD_CLK pin is configured as an input. A '0' indicates the AUDCLKDIV field of the BUS_CHPCNTL register is used to control by what value SPOT uses to divide the AUD_XTALI input by in order to then drive the AUD_CLK pin on the chip.
16	VIDCLKSRC	A '0' in this field indicates the clock for the video encoder originates external to the SPOT chip. and the VID_PIXCLK and VID_PIX2XCLK pins are configured as inputs. A '1' indicates the video clocks originate from the SPOT chip. They are divided down from the VID_4XXTALI input.
15:14	CPUMULT[1:0]	This field indicates the clock multiplier which should be programmed into the CPU upon reset. During reset, these values are sent to the CPU so it can configure its internal PLL to use the clock multiplier outlined in the table below.
13	CPUBUFF	When '1', this field tells the SPOT CPU reset logic to configure the CPU's output buffers to 50% strength. A '0' indicates to configure to 83%. NOTE: double-check.
12	RESERVED	Reserved for future use.
11	NTSC	A '1' in this field indicates the system is configured for NTSC mode. and a 12.27MHz pixel clock A '0' indicates PAL mode and a 14.75MHz pixel clock.
10:8	RESERVED	Reserved for future use.
7:4	BRDREV[3:0]	This field indicates the revision of the board type. The revision field starts at 0b1111 and counts down.

3:2	BRDTYP[1:0]	This field indicates the board type. See tables below for encoding.
1:0	RESERVED	Reserved for future use.

Following are the encoding tables of the fields in the previous table.

Table 4-16 ROMSPDx Encoding

ROMSPDx[1:0]	Encoding (Initial Access/Page Access)
0b00	200ns/100ns
0b01	100ns/50ns
0b10	90ns/45ns
0b11	120ns/60ns

Table 4-17 MEMSPD Encoding

MEMSPD[1:0]	Encoding
0b00	100MHz parts
0b01	66MHz parts
0b10	77MHz parts
0b11	83MHz parts

MEMVEND Encoding

MEMVEND[1:0]	Encoding
0b00	Other
0b01	Samsung
0b10	Fujitsu
0b11	NEC

Table 4-18 AUDDACTYP Encoding

AUDDACTYP[1:0]	Encoding
0b00 - 0b10	reserved
0b11	AKM 4310/4309

CPUMULT Encoding

CPUMULT[1:0]	Encoding
0b00	CPU clock = 5X bus clock
0b01	CPU clock = 4X bus clock
0b10	CPU clock = 2X bus clock
0b11	CPU clock = 3X bus clock

Table 4-19 BRDTYP Encoding

BRDTYP [1:0]	Encoding
0b00 - 0b01	reserved
0b10	Trial-type board
0b11	FCS board

4.2.2.2 ROM_CNTL0 Register

This register is used to program the state machine which accesses the ROM bank 0 parts in the system. Software should set this register after querying the ROM_SYSCONFIG register.

Table 4-20 ROM_CNTL0 Bit Definition

Bits	Symbol	Meaning
31	ROMPAGE	When '1', this bit indicates ROM bank contains page-mode ROMs. If '0', the romUnit state machine decoding ROM bank will use INITWAIT field for all accesses. After reset, this bit is '0'.
30:29	RESERVED	Reserved for future use.
28:24	PAGEWAIT[4:0]	This field indicates how many clock cycles the state machine controlling ROM bank should wait between page mode accesses before latching data. Aftrer reset, this field contains 0b11111.
23:21	RESERVED	Reserved for future use.
20:16	INITWAIT[4:0]	This field indicates how many clock cycles the state machine controlling ROM bank should wait on the initial access before latching data. Aftrer reset, this field contains 0b11111.
15	RESERVED	Reserved for future use.
14:12	CEDEL[2:0]	This field indicates how many clock cycles the state machine controlling ROM bank should deassert CE for between accesses. Aftrer reset, this field contains 0b111.
11:10	RESERVED	Reserved for future use.
9:8	WEDEL[1:0]	This field indicates how many clock cycles the state machine controlling ROM bank should wait after ROM_CE_N's assertion to assert ROM_WE_N. Aftrer reset, this field contains 0b11.
7:4	RESERVED	Reserved for future use.
3:0	WETIME0[3:0]	This field indicates how many clock cycles the state machine controlling ROM bank should assert ROM_WE_N for during a write to bank. Aftrer reset, this field contains 0b1111. Note that software should never program WEDELx + WETIMEx to be greater than INITWAITx.

4.2.2.3 ROM_CNTL1 Register

This register is used to program the state machine which accesses the ROM bank 1 parts in the system. Software should set this register after querying the ROM_SYSCONFIG register.

Table 4-21 ROM_CNTL1 Bit Definition

Bits	Symbol	Meaning
31	ROMPAGE	When '1', this bit indicates ROM bank contains page-mode ROMs. If '0', the romUnit state machine decoding ROM bank will use INITWAIT field for all accesses. After reset, this bit is '0'.
30:29	RESERVED	Reserved for future use..
28:24	PAGEWAIT[4:0]	This field indicates how many clock cycles the state machine controlling ROM bank should wait between page mode accesses before latching data. Aftrer reset, this field contains 0b11111.
23:21	RESERVED	Reserved for future use..
20:16	INITWAIT[4:0]	This field indicates how many clock cycles the state machine controlling ROM bank should wait on the initial access before latching data. Aftrer reset, this field contains 0b11111.
15	RESERVED	Reserved for future use..
14:12	CEDEL[2:0]	This field indicates how many clock cycles the state machine controlling ROM bank should deassert CE for between accesses. Aftrer reset, this field contains 0b111.
11:10	RESERVED	Reserved for future use..
9:8	WEDEL[1:0]	This field indicates how many clock cycles the state machine controlling ROM bank should wait after ROM_CE_N's assertion to assert ROM_WE_N. Aftrer reset, this field contains 0b11.
7:4	RESERVED	Reserved for future use..
3:0	WETIME0[3:0]	This field indicates how many clock cycles the state machine controlling ROM bank should assert ROM_WE_N for during a write to bank. Aftrer reset, this field contains 0b1111. Note that software should never program WEDELx + WETIMEx to be greater than INITWAITx.

4.2.3 audUnit Registers

4.2.3.1 AUD_CSTART Register

This register is used to set and view the starting byte address of the currently executing DMA transfer.

Table 4-22 AUD_CSTART Bit Definition

Bits	Symbol	Meaning
31:26	RESERVED	Reserved for future use.
25:0	CADDR[25:0]	This field reflects the value of the starting address of the current DMA transaction.

4.2.3.2 AUD_CSIZE Register

This register is used to set and view the size of the curently executing DMA transfer. Note that audio DMA transfers can only be up to 64KB.

Table 4-23 AUD_CSIZE Bit Definition

Bits	Symbol	Meaning
31:16	RESERVED	Reserved for future use.
15:0	CSIZE[15:0]	This field reflects the value of the size of the current DMA transaction.

4.2.3.3 AUD_CCONFIG Register

This register is used to control the sample sizes and mono vs. stereo in the currently executing audio DMA channel.

Table 4-24 AUD_CCONFIG Bit Definition

Bits	Symbol	Meaning
31:2	RESERVED	Reserved for future use.
1	8BIT	When '1', this bit indicates the audio samples should be 8-bit. When '0', 16-bit samples are used. After reset, this bit is undefined.
0	MONO	When '1', this bit indicates mono samples should be used. When '0', stereo samples are being used in the audio DMA channel. After reset, this bit is undefined

4.2.3.4 AUD_CCNT Register

This register is used to to view the (byte) count of the curently executing DMA transfer

Table 4-25 AUD_CCNT Bit Definition

Bits	Symbol	Meaning
31:16	RESERVED	Reserved for future use.
15:0	CCNT[15:0]	This field reflects the value of the index count of the current DMA transaction. Software can determine how far along the DMA transfer is by reading this register.

4.2.3.5 AUD_NSTART Register

This register is used to read and write the starting address of the next DMA transfer.

Table 4-26 AUD_NSTART Bit Definition

Bits	Symbol	Meaning
30:26	RESERVED	Reserved for future use.
25:0	NADDR[25:0]	This field reflects the value of the starting address of the next DMA transaction.

4.2.3.6 AUD_NSIZE Register

This register is used to to read and write the size of the next DMA transfer.

Table 4-27 AUD_NSIZE Bit Definition

Bits	Symbol	Meaning
31:16	RESERVED	Reserved for future use.
15:0	NSIZE[15:0]	This field reflects the value of the size of the next DMA transaction.

4.2.3.7 AUD_NCONFIG Register

This register is used to control the sample sizes and mono vs. stereo in the "next" executing audio DMA channel.

Table 4-28 AUD_NCONFIG Bit Definition

Bits	Symbol	Meaning
31:2	RESERVED	Reserved for future use.
1	8BIT	When '1', this bit indicates the audio samples should be 8-bit. When '0', 16-bit samples are used. After reset, this bit is undefined.
0	MONO	When '1', this bit indicates mono samples should be used. When '0', stereo samples are being used in the audio DMA channel. After reset, this bit is undefined.

4.2.3.8 AUD_DMACNTL Register

This register is used to control the audio DMA channel.

Table 4-29 AUD_DMACNTL Bit Definition

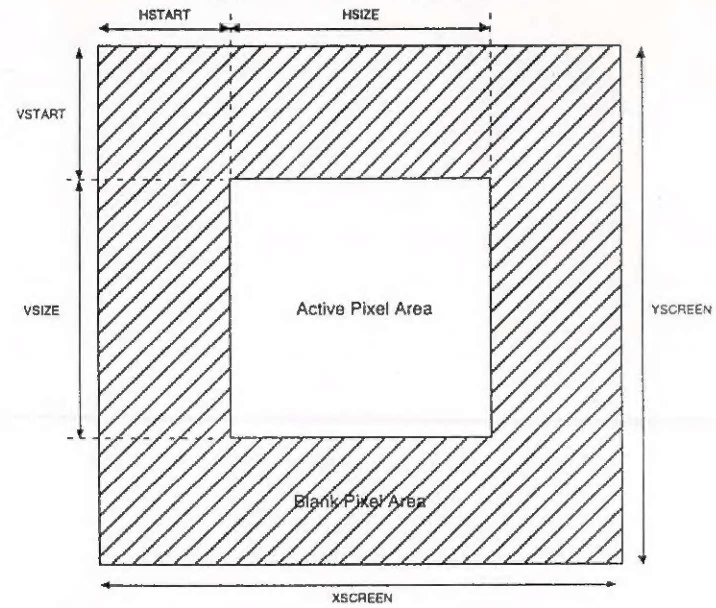
Bits	Symbol	Meaning
31:3	RESERVED	Reserved for future use.
2	DMAEN	When '1', this bit indicates the DMA channel is enabled. When '0', the DMA channel is disabled. After reset this bit is '0'. A '1' to '0' transition on this bit will flush the current DMA transaction (i.e. the channel will be reset).
1	NV	When '1', this bit indicates the NSTART and NSIZE registers are valid. Software should first set up the "next" registers, then enable the NV bit, and finally set the DMAEN bit in order to start the DMA channel.
0	NVF	When '1', this bit indicates the NV should stay valid forever. This allows software to have a continuous loop on a buffer such as an audio sample.

4.2.4 vidUnit Registers

4.2.4.1 vidUnit Programming Overview

The vidUnit in SPOT can drive both interlace and non-interlace NTSC or PAL displays. There are several registers which control the various features of the vidUnit plus control the actual frame being displayed on the screen. Both the horizontal and veritical resolution of the video display are programmable. The picture below outlines several vidUnit parameters which are key to understanding how the video display operates.

Figure 4-1 Video Display Overview



The vidUnit is basically a DMA engine which reads the frame buffer from main memory and displays to the screen. A TV has a resolution of 'X' pixels by 'Y' lines. For NTSC, X=640 and Y=480, but not all of these pixels are visible since they are in the blank time or in the overscan region of the TV. SPOT allows software to position the active window anywhere onto the overall X and Y coordinates of the TV such that all pixels will be guaranteed to be visible. This is done by programming the HSTART, HSIZE, VSTART, and VSIZE registers in SPOT. As long as the DMA size is set exactly to the size of the active pixel area, the vidUnit will continuously display the frame buffer to the TV each field (for interlace) or each frame (for non-interlace).

There is a definite sequence of events software must follow in order to enable video. The rules are outlined below:

Non-Interlace Video

1) Set up the DMA registers VID_NSTART and VID_NSIZE. NSIZE must be set to: (HSIZE*VSIZE)*2
2) Set the NV and NVF bits of the VID_DMACNTL register. Make sure the INTERLACEEN bit of this register is set to '0'.
3) Set the DMAEN bit of the VID_DMACNTL register
4) Set the HSTART, HSIZE, VSTART, and VSIZE registers. HSTART must be a multiple of '2'. HSIZE must be a multiple of 8 pixels (4 words). Make sure enough time has elapsed to allow the DMA engine to pre-load the video pixel buffer. This will be approximately 100 system clock cycles.

Table 4-36 VID_DMACNTL Bit Definition

Bits	Symbol	Meaning
31:4	RESERVED	Reserved for future use.
3	DMAINTERLACEEN	When '1', this bit indicates the DMA channel will support interlaced video depending on the value of HSIZE and VSIZE. When '0', the DMA channel supports non-interlace mode. After reset this bit is '0'
2	DMAEN	When '1', this bit indicates the DMA channel is enabled. When '0', the DMA channel is disabled. After reset this bit is '0'. A '1' to '0' transition on this bit will flush the current DMA transaction (i.e. the channel will be reset).
1	NV	When '1', this bit indicates the NSTART and NSIZE registers are valid. Software should first set up the "next" registers, then enable the NV bit, and finally set the DMAEN bit in order to start the DMA channel. When shutting down DMA, SW must first turn off the display and wait for 2 VSYNC's to elapse before then shutting down DMA. For SPOT1, this bit really has no meaning as far as chaining is concerned. Once video has been enabled, the DMA engine will continue re-loading regardless of the NV or NVF bits. :-)
0	NVF	When '1', this bit indicates the NV should stay valid forever. This allows software to have a continuous loop on a buffer such as a video frame.

4.2.4.9 VID_FCNTL Register

This register is used to control miscellaneous modes of the video DMA channel.

Table 4-37 VID_FCNTL Bit Definition

Bits	Symbol	Meaning
31:8	RESERVED	Reserved for future use.
7	UVSELSWAP	When '1', this bit indicates that the vidUnit will support YCbYCr pixel format when using a Bt851 video encoder in the system. When '0', YCrYCb format is supported for this video encoder.
6	CRCBINVERT	When '1', this bit indicates that the vidUnit should invert the MSB of Cr and Cb values coming from memory before passing on to the video encoder. After reset this bit is '0'.
5	FIDO	When '1', this bit indicates the vidUnit should be in "FIDO" mode. After reset this bit is '0'. FIDO mode is TBD (Beth will fill in here)
4	GAMMA	When '1', this bit indicates gamma correction should be done to all pixels passing through the unit. A '0' disables gamma correction.
3	BLNKCOLEN	When '1', this bit indicates the blank color register should be enabled on the output during "blank" times instead of just asserting the VID_BLANK signal and getting black output. After reset this bit is '0'.
2	INTERLACE	When '1', this bit indicates the vidUnit is configured for interlace mode. This bit is also reflected out on the VID_CNTL[0] signal of the chip. This signal should be connected to the INTERLACE pin on the video encoder. After reset, this bit is '0'
1	PAL	When '1', this bit indicates the vidUnit is configured for PAL mode. This bit is also reflected out on the VID_CNTL[1] signal of the chip. This signal should be connected to the PAL pin on the video encoder. After reset, this bit is initialized with the value of the inverted bit in the ROM_SYSCONFIG register. It can be overwritten after reset with any value
0	VIDENAB	When '1', this bit indicates the video subsystem should start displaying screens. Video is is either disabled or the color values contained in the VID_BLNKCOL register are displayed during pixel times if BLNKCOLEN is '1' when VIDENAB is '0'. The DMA channel needs to be set up prior to the VIDENAB bit being set. After reset this bit is '0'.

4.2.4.10 VID_BLNKCOL Register

This register is used to set the default color value to be displayed if this feature is enabled

Table 4-38 VID_BLNKCOL Bit Definition

Bits	Symbol	Meaning
31:24	RESERVED	Reserved for future use.
23:16	YCOL	Y value to be displayed for each pixel during blank times.
15:8	CRCOL	Cr value to be displayed for each pixel during blank times.
7:0	CBCOL	Cb value to be displayed for each pixel during blank times.

4.2.4.11 VID_HSTART Register

This register is used to set the horizontal starting position of active pixels on the screen. The value in this register plus the values in the HSIZE, VSTART, and VSIZE need to match the appropriate DMA buffer size that software must set up (i.e. hardware does not check that all values jive).

Table 4-39 VID_HSTART Bit Definition

Bits	Symbol	Meaning
31:10	RESERVED	Reserved for future use.
9:0	HSTART[9:0]	This field reflects the horizontal starting pixel out of the possible 640 (NTSC) or 768 (PAL). Must start on an even boundary (i.e. multiple of '2'). Note that this value counts '0'. Thus, if '2' is put in this register then the active display will start on the 3rd pixel (0, 1, 2).

4.2.4.12 VID_HSIZE Register

This register is used to set the horizontal pixel size of the screen.

Table 4-40 VID_HSIZE Bit Definition

Bits	Symbol	Meaning
31:10	RESERVED	Reserved for future use.
9:0	HSIZE[9:0]	This field reflects the horizontal screen size of the active area. The HSTART + HSIZE value must not be greater than 640 (NTSC) or 768 (PAL) or unpredictable results will occur. The actual "safe" horizontal area for NTSC is 540 while it is 640 for PAL. Must be a multiple of 8 pixels (4 words).

4.2.4.13 VID_VSTART Register

This register is used to set the vertical starting position of active lines on the screen. The value in this register plus the values in teh HSIZE, HSTART, and VSIZE need to match the appropriate DMA buffer size that software must set up (i.e. hardware does not check that all values jive).

Table 4-41 VID_VSTART Bit Definition

Bits	Symbol	Meaning
31:10	RESERVED	Reserved for future use.
9:0	VSTART[9:0]	This field reflects the vertical starting line out of the possible 525 (NTSC) or 625 (PAL). Note that this register does not count '0'. If '2' were written into this register then the active pixels would start on the second line (1,2).

4.2.4.14 VID_VSIZE Register

This register is used to set the number of lines on the screen. In interlace mode, this field reflects field lines, not frame lines.

Table 4-42 VID_VSIZE Bit Definition

Bits	Symbol	Meaning
31:10	RESERVED	Reserved for future use.
9:0	VSIZE[9:0]	This field reflects the vertical size of the active area The VSTART + VSIZE value must not be greater than 525 (NTSC) or 625 (PAL) or unpredictable results will occur. The actual "safe" vertical area for NTSC is 420 while it is 480 for PAL. In interlace mode, this field indicates field lines and not frame lines. Thus, SW should program this to 1/2 desired frame size

4.2.4.15 VID_HINTLINE Register

This register is used to set the line which will generate an interrupt if the VIDHSYNCEN bit is set in the VID_INTEN register.

Table 4-43 VID_ HINTLINE Bit Definition

Bits	Symbol	Meaning
31:10	RESERVED	Reserved for future use.
9:0	HINTLINE[9:0]	This field reflects the line which will cause the interrupt if the horizontal interrupt is enabled. After reset, this field is 0x000.

4.2.4.16 VID_CLINE Register

This register is used to read the current line being displayed.

Table 4-44 VID_ CLINE Bit Definition

Bits	Symbol	Meaning
31:11	RESERVED	Reserved for future use.
10:0	CLINE[10:0]	This field reflects the line which is currently being displayed. Note that CLINE[10] indicates whether or not the current line is in an odd field (1) or an even field (0)

4.2.4.17 VID_INTSTAT Register

This register (register pair) provides the status of any video interrupt generated within SPOT. Whenever an interrupt is detected by the enable being set and video interrupting, SPOT will assert the CPU_INT_N signal and keep it asserted until the source of the interrupt is disabled.

Table 4-45 VID_INTSTAT Bit Definition

Bits	Symbol	Meaning
31:6	RESERVED	Reserved for future use.
6	VIDFIDO	When this bit is set to '1', a vidUnit interrupt has occurred due to a FIDO event taking place. This is to be filled out later. Clearing the interrupt is done by writing a '1' to the corresponding bit in the VID_INTSTAT _C register.
5	VIDVSYNCE	When this bit is set to '1', a vidUnit interrupt has occurred due to a vertical sync indicating the start of an even field. Clearing the interrupt is done by writing a '1' to the corresponding bit in the VID_INTSTAT _C register
4	VIDVSYNCO	When this bit is set to '1', a vidUnit interrupt has occurred due to a vertical sync indicating the start of an odd field Clearing the interrupt is done by writing a '1' to the corresponding bit in the VID_INTSTAT _C register.
3	VIDHSYNC	When this bit is set to '1', a vidUnit interrupt has occurred due to a horizontal sync occuring on line 'n' where 'n' is the line defined in the VID_HINTLINE register. It is the HSYNC after the HINTLINE is displayed which triggers this interrupr. Clearing the interrupt is done by writing a '1' to the corresponding bit in the VID_INTSTAT _C register
2	VIDDMA	When this bit is set to '1', a vidUnit interrupt has occurred due to the current video DMA channel completing. Clearing the interrupt is done by writing a '1' to the corresponding bit in the VID_INTSTAT _C register.
1:0	RESERVED	Reserved for future use. These bit s will read back as '0'

4.2.4.18 VID_INTEN Register

This register (register pair) provides the status of any video interrupt generated within SPOT. Whenever an interrupt is detected by the enable being set and video interrupting, SPOT will assert the CPU_INT_N signal and keep it asserted until the source of the interrupt is disabled.

Table 4-46 VID_ INTEN Bit Definition

Bits	Symbol	Meaning
31:6	RESERVED	Reserved for future use.
6	VIDFIDOEN	When '1', this bit enables FIDO video interrupts to pass through and be seen by the CPU. When '0', this interrupt source is disabled. Software must write a '1 to VID_INTEN_S location to set the bit and write a '1 to the VID_INTEN _C location to clear the bit. This bit is set to '0 after reset.
5	VIDVSYNCEEN	When '1', this bit enables even-field vertical sync interrupts to pass through and be seen by the CPU When '0', this interrupt source is disabled. Software must write a '1 to VID_INTEN_S location to set the bit and write a '1' to the VID_INTEN _C location to clear the bit. This bit is set to '0 after reset.
4	VIDVSYNCOEN	When '1', this bit enables odd-field vertical sync interrupts to pass through and be seen by the CPU When '0', this interrupt source is disabled. Software must write a '1 to VID_INTEN_S location to set the bit and write a '1' to the VID_INTEN _C location to clear the bit. This bit is set to '0 after reset
3	VIDHSYNCEN	When '1', this bit enables horizontal sync interrupts to pass through and be seen by the CPU When '0', this interrupt source is disabled. Software must write a '1 to VID_INTEN_S location to set the bit and write a '1' to the VID_INTEN _C location to clear the bit This bit is set to '0 after reset.
2	VIDDMAEN	When '1', this bit enables video DMA interrupts to pass through and be seen by the CPU When '0', this interrupt source is disabled. Software must write a '1 to VID_INTEN_S location to set the bit and write a '1 to the VID_INTEN _C location to clear the bit This bit is set to '0 after reset.
1:0	RESERVED	Reserved for future use. These bit s will read back as '0'

4.2.5 devUnit Registers

4.2.5.1 DEV_IRDATA Register

This register is used to read the input data from the IR controller.

Table 4-47 DEV_IRDATA Bit Definition

Bits	Symbol	Meaning
31:0	IRDATA[31:0]	This field contains the IR input data stream (32-bits)

4.2.5.2 DEV_LED Register

This register is used to control the 3 LEDs in the system.

Table 4-48 DEV_LED Bit Definition

Bits	Symbol	Meaning
31:3	RESERVED	Reserved for future use.
2	LED[2]	This bit controls the LED connected to the MISC_LED[2] signal on the chip. This LED indicates "power on". A '0' turns the LED on. A '1' turns the LED off After reset, this bit is '1'.
1	LED[1]	This bit controls the LED connected to the MISC_LED[1] signal on the chip. This LED indicates "modem connected". A '0' turns the LED on. A '1' turns the LED off After reset, this bit is '1'.
0	LED[0]	This bit controls the LED connected to the MISC_LED[0] signal on the chip. This LED indicates "modem connected" A '0' turns the LED on. A '1' turns the LED off After reset, this bit is '1'

4.2.5.3 DEV_IDCNTL Register

This register is used to control the unique ID chip in the system

Table 4-49 DEV_IDCNTL Bit Definition

Bits	Symbol	Meaning
31:2	RESERVED	Reserved for future use.
1	IDDATAO	This bit is used to drive the ID data line. A '1' written to the bit reflects a '1' on the ID_DATA signal (open drain driver on chip) while a '0' reflects a '0' on the ID_DATA line. Software must make sure this bit is '1' when attempting to read the IDDATAI bit. After reset this bit is '1'.
0	IDDATAI	Software can read this bit to see what the "live" value of the ID_DATA signal is. Writes have no effect to this bit

4.2.5.4 DEV_NVCNTL Register

This register is used to control the EEPROM chip (NVRAM) in the system.

Table 4-50 DEV_NVCNTL Bit Definition

Bits	Symbol	Meaning
31:4	RESERVED	Reserved for future use.
3	NVCLK	This bit is directly reflected on the EEP_CLK signal of the chip. Software writes '1' and '0' to this bit to clock the EEPROM chip.. After reset this bit is '0'
2	NVDATAOEN	A '1' in this field enables the output buffer for the EEP_DATA signal and the SPOT chip will drive the value in the NVDATAO field on this signal A '0' in this field will tri-state the EEP_DATA signal. After reset this field is '0'.
1	NVDATAO	This value of this field is driven out on the EEP_DATA signal when the NVDATAOEN is '1 This is used to write data to the NVRAM part
0	NVDATAI	This field is used to read the value on the EEP_DATA signal This is used to read data from the NVRAM part. Writes to this field have no effect

4.2.5.5 DEV_SCCNTL Register

This register is used to control the SmartCard interface in the system.

Table 4-51 DEV_SCCNTL Bit Definition

Bits	Symbol	Meaning
31:6	RESERVED	Reserved for future use.
5	SCCLK	This bit is directly reflected on the SMC_CLK signal of the chip. Software writes '1' and '0' to this bit to clock the SmartCard. After reset this bit is '0'
4	SCDATAOEN	A '1' in this field enables the output buffer for the SMC_DATA signal and the SPOT chip will drive the value in the SCDATAO field on this signal. A '0' in this field will tri-state the SMC_DATA signal. After reset this field is '0'
3	SCDATAO	This value of this field is driven out on the SMC_DATA signal when the SCDATAOEN is '1' This is used to write data to the SmartCard
2	SCDATAI	This field is used to read the value on the SMC_DATA signal. This is used to read data from the SmartCard Writes to his field have no effect.
1	SCRESET	This bit is directly reflected on the SMC_RESET signal of the SPOT chip. After reset this bit is '0'
0	SCINSERT	This bit directly reflects the value present on the SMC_INSERT signal of the SPOT chip. This is a read-only bit field and writes to it have no effect. This bit can be useful to filter spurious inserts on the SmartCard connector Writes to his field have no effect.

4.2.5.6 DEV_EXTTIME Register

This register is used to control the timing of the accesses to the external keyboard or modem controllers.

Table 4-52 DEV_EXTTIME Bit Definition

Bits	Symbol	Meaning
31:28	KBDCSTIME	This field indicates how many SYS_CLK cycles the KBD_CS_N signal is help asserted for during a read or write to one of the 8 keyboard-space registers. After reset, this field is set to 0xF.
27:24	KBDWRTIME	This field indicates how many SYS_CLK cycles the IO_WR_N signal is held asserted for during a write or how many SYS_CLK cycles the IO_RD_N signal is active during a read when accessing one of 8 keyboard-space registers. After reset, this field is set to 0x8.
23:22	KBDWRDEL	This field indicates how many SYS_CLK cycles to delay the assetion of IO_WR_N from the assertion of KBD_CS_N during a write or how many SYS_CLK cycles to delay the assetion of IO_RD_N from the assertion of KBD_CS_N during a read when accessing one of 8 keyboard-space registers. After reset, this field is set to 0x2.
21:16	RESERVED	Reserved for future use.
15:12	MODCSTIME	This field indicates how many SYS_CLK cycles the MOD_CS_N signal is help asserted for during a read or write to one of the 8 modem-space registers. After reset, this field is set to 0xF.
11:8	MODWRTIME	This field indicates how many SYS_CLK cycles the IO_WR_N signal is held asserted for during a write or how many SYS_CLK cycles the IO_RD_N signal is active during a read when accessing one of 8 modem-space registers. After reset, this field is set to 0x8.
7:6	MODWRDEL	This field indicates how many SYS_CLK cycles to delay the assetion of IO_WR_N from the assertion of KBD_CS_N during a write or how many SYS_CLK cycles to delay the assetion of IO_RD_N from the assertion of KBD_CS_N during a read when accessing one of 8 modem-space registers. After reset, this field is set to 0x2.
5:0	RESERVED	Reserved for future use.

4.2.5.7 DEV_KBDn Registers

These 8 registers are used to send data to/from the external keyboard controller chip. When this space is selected, the KBD_CS_N signal on SPOT activates plus the IO_ADDR[2:0] signals reflect the values present on Address[4:2]. The IO_RD_N and IO_WR_N signals of the chip are activated based on a CPU read or write of these registers. The timing of the accesses to the external keyboard controller chip is controlled by the fields in the DEV_EXTTIME register.

Table 4-53 DEV_KBDn Bit Definition

Bits	Symbol	Meaning
31:8	RESERVED	Reserved for future use.
7:0	KBDDATA[7:0]	This field contains the data which is placed on the IO_DATA[7:0] signals of the chip son writes and which reads the value of the IO_DATA[7:0] bus on reads.

4.2.5.8 DEV_MODn Registers

These 8 registers are used to send data to/from the external modem chip. When this space is selected, the MOD_CS_N signal on SPOT activates plus the IO_ADDR[2:0] signals reflect the values present on Address[4:2]. The IO_RD_N and IO_WR_N signals of the chip are activated based on a CPU read or write of these registers. The timing of the accesses to the external modem chip is controlled by the fields in the DEV_EXTTIME register.

Table 4-54 DEV_MODn Bit Definition

Bits	Symbol	Meaning
31:8	RESERVED	Reserved for future use.
7:0	MODDATA[7:0]	This field contains the data which is placed on the IO_DATA[7:0] signals of the chip son writes and which reads the value of the IO_DATA[7:0] bus on reads.

4.2.6 memUnit Registers

4.2.6.1 MEM_CNTL Register

This register is used to control various features of the memory controller.

Table 4-55 MEM_CNTL Bit Definition

Bits	Symbol	Meaning
31:30	MEMCL[1:0]	This field is used to tell the memUnit what the CAS latency was set to on a previous SGRAM MODE register set command (MRS). See table below for encoding. After reset, this field is 0b11.
29:0	RESERVED	Reserved for future use.

Table 4-56 MEMCL Encoding

MEMCL[1:0]	Encoding
0b00	reserved
0b01	CAS latency was set to '1' in SGRAM
0b10	CAS latency was set to '2' in SGRAM
0b11	CAS latency was set to '3' in SGRAM

4.2.6.2 MEM_REFCNT Register

This register is used to set the refresh counter timing in the memory controller.

Table 4-57 MEM_REFCNT Bit Definition

Bits	Symbol	Meaning
31:14	RESERVED	Reserved for future use.
13:0	MEMRFCNT[13:0]	This field is used to set thow many SYS_2XCLK cycles elapse between SGRAM memory refreshes. After reset, this field is set to 0x0400. The ideal value in this field is whatever makes the refresh interval 16μs based on the system clock frequency (recall software will determine system clock frequency via video interrupts).

4.2.6.3 MEM_DATA Register

This register is used to send specific data patterns to the SGRAMs during various commands.

Table 4-58 MEM_DATA Bit Definition

Bits	Symbol	Meaning
31:0	MEMDATA[31:0]	This field is sent out on each memory command operation. A memory command is issued by software writing to the MEM_CMD register. When a command is sent, the MEM_DATA bus on the SPOT chip gets driven with the contents of this MEM_DATA register.

4.2.6.4 MEM_CMD Register

This register is used to send commands to the SGRAM parts. The upper bits of the address select which SGRAM parts are sent the command if there is more than one SGRAM part in the system. It is crucial software write this register after reset in order to get the SGRAMs into an operational mode. The required power-upreset sequence is:

1) write 0xc000_0000 to MEM_CNTL register (CAS Latency set to '3')
2) write 0xADBA_C024 to MEM_TIMING (set timing parameters)
3) write 0x0000_???? to MEM_REFCNT (make 16us - dependent upon CPU frequency)
4) write 0x0000_0000 to MEM_DATA
5) write 0x8800_0000 to MEM_CMD (Precharge all banks of all chips)
6) write 0x4800_0000 to MEM_CMD (Refresh all chips)
7) write 0x4800_0000 to MEM_CMD (Refresh all chips)
8) write 0x4800_0000 to MEM_CMD (Refresh all chips)
9) write 0x4800_0000 to MEM_CMD (Refresh all chips)
10) write 0x4800_0000 to MEM_CMD (Refresh all chips)
11) write 0x4800_0000 to MEM_CMD (Refresh all chips)
12) write 0x4800_0000 to MEM_CMD (Refresh all chips)
13) write 0x4800_0000 to MEM_CMD (Refresh all chips)
14) write 0x2800_00C0 to MEM_CMD (write mode register with CL=3 (all chips))
15) write 0x8800_0000 to MEM_CMD (Precharge all banks of all chips)

Table 4-59 MEM_CMD Bit Definition

Bits	Symbol	Meaning
31:28	MEMCMD[3:0]	This field is used to send a command to the SGRAM part(s). The table below shows the encoding. This field is write-only.
27	MEMALLCHIPS	Issue command to all chips when '1'. Note it is illegal to have this bit '1' when performing a READ/WRITE, or BW command.
29:26	RESERVED	Reserved for future use.
25:0	MEMADDR[25:0]	This field contains the address to which the SGRAM command is performed upon. The upper bits of the address indicate which SGRAM gets the command.

Table 4-60 MEMCMD Encoding

Table 4-61

MEMCMD[3:0]	OPCODE	Encoding
0x0	PRE	Precharge
0x1	ACT	Activate
0x2	MRS	Mode Register Set
0x3	SRS	Special Register Set
0x4	REF	Refresh
0x5	READ	Read
0x6	WRITE	Write
0x7	BW	Block Write
0x8	PALL	Precharge All Banks
0x9	PD_ENTRY	Power-down Entry
0xa	PD_EXIT	Power-down Exit
0xb	SUSP_ENTRY	Clock Suspend Entry
0xc	SUSP_EXIT	Clock Suspend Exit
0xd	SELF_ENTRY	Self-refresh Power-down Entry
0xe	SELF_EXIT	Self-refresh Power-down Exit
0xf	RESERVED	Reserved for future use.

4.2.6.5 MEM_ TIMING Register

This register is used to set up various timing parameters in the memUnit. The values which are written into these fields is dependent upon:

1) frequency of memory operation
2) memory vendor
3) memory speed grade
4) CAS latency

Table 4-62 MEM_TIMING Bit Definition

Bits	Symbol	Meaning
31:29	MEMTRTW[2:0]	Read to write time. Reset to 0x5.
28:27	MEMTRTP[1:0]	Read/Write to Precharge time. Reset to 0x1.
26:25	MEMTRSC[1:0]	Mode Register set cycle time. Reset to 0x2.
24:22	MEMTBAL[2:0]	Block write data-in to REF/ACT Cmd. Reset to 0x6.
21:20	MEMTBPL[1:0]	Block write data-in to PRE Cmd. Reset to 0x3.
19:18	MEMTBWC[1:0]	Block write cycle time. Reset to 0x2.
17:15	MEMTDAL[2:0]	Write data-in to PRE Cmd. Reset to 0x5.
14:13	MEMTDPL[1:0]	Write data-in to REF/ACT Cmd. Reset to 0x2.
12:11	MEMTRRD[1:0]	ACT0 to ACT1 command period. Reset to 0x3.
10:9	MEMTRCD[1:0]	ACT to R/W delay time. Reset to 0x3.
8:7	MEMTRP[1:0]	PRE to REF/ACT comand period. Reset to 0x3.
6:4	MEMTRAS[2:0]	PRE/ACT to PRE command period. Reset to 0x7.
3:0	MEMTRC[3:0]	REF to REF/ACT command period. Reset to 0xa.

4.3 DMA Interface

The audio and video DMA engines are each built around the same DMA interface. Transfers are done from a logical block in memory defined by a word aligned start address and a buffer size in words. Two sets of registers are maintained, one for the active buffer and one for the next buffer which may not be valid. DMA transfers are started by loading a start address and buffer size into the next buffer registers, asserting the next buffer valid bit and then asserting the DMA enable control bit.

The DMA engine will transfer the next buffer information into the read–only registers of the active buffer and de–assert the next buffer valid bit. A counter will begin counting up to the size of the active buffer and incrementing memory addresses as accesses are requested from the memory. The current state of the buffer is readable through the engines' control registers including start address, buffer size, and the index of the last access. When the engine has completed the last access in the current buffer, it will assert an interrupt alerting the CPU that the buffer is now exhausted.

DMA chaining is implemented by both engines. When the current buffer has been exhausted, the engine will check the next buffer valid bit. If this bit is set, the next buffer information will be transferred to the active buffer, the valid bit will be cleared and transfers will continue from the newly active buffer. This process will continue until the DMA enable control bit is explicitly de–asserted by the CPU or until the active buffer is exhausted and the next buffer valid bit is not set. In this condition, the engine will automatically de–assert the enable bit and halt DMA transactions.

Figure 4-2 DMA Engine Control

(put diagram here)

5) Set the various control bits in the VID_FCNTL register such as CRCBSWAP, CRCBINVERT, BLNKCOLEN. Make sure the INTERLACE bit of this register is set to '0'.
6) Set the VIDENAB bit in the VID_FCNTL register

Interlace Video

1) Set the HSTART, HSIZE, VSTART, and VSIZE registers. HSTART must be a multiple of '2'. HSIZE must be a multiple of 8 pixels (4 words). VSIZE must be 1/2 of actual vertical line size.
2) Set up the DMA registers VID_NSTART and VID_NSIZE. VID_NSIZE must be set to: (HSIZE*VSIZE)*2
3) Set the NV and NVF bits of the VID_DMACNTL register. Make sure the INTERLACEEN bit of this register is set to '1'.
4) Set the DMAEN bit of the VID_DMACNTL register
5) Make sure enough time has elapsed to allow the DMA engine to pre-load the video pixel buffer. This will be approximately 100 system clock cycles.
6) Set the various control bits in the VID_FCNTL register such as CRCBSWAP, CRCBINVERT, BLNKCOLEN. Make sure the INTERLACE bit of this register is set to '1'.
7) Set the VIDENAB bit in the VID_FCNTL register

4.2.4.2 Pixel Format

The pixel format within memory is as outlined in the table below.

Table 4-30 Pixel Format in Memory

Bits	Symbol	Meaning
31:24	Y	Luminance value for pixel 'n'.
23:16	C_b	Chrominance (blue) value for pixel 'n' and 'n+1'.
15:8	Y	Luminance value for pixel 'n+1'
7:0	C_r	Chrominance (red) value for pixel 'n' and 'n+1'.

It should be noted for SPOT1 memory can be orgranized YCrYCb as long as the UVSELSWAP bit in VID_FCNTL is set to '0'. Future video encoders such as Philips and Bt852 will require YCbYCr.

4.2.4.3 VID_CSTART Register

This register is used to set and view the starting word address of the currently executing video DMA transfer.

Table 4-31 VID_CSTART Bit Definition

Bits	Symbol	Meaning
31:25	RESERVED	Reserved for future use.
26:0	CADDR[26:0]	This field reflects the value of the starting address of the current DMA transaction. IF CADDR[26] = '1', ROM space is accesses as opposed to main memory.

4.2.4.4 VID_CSIZE Register

This register is used to view the size (in bytes) of the curently executing DMA transfer.

Table 4-32 VID_CSIZE Bit Definition

Bits	Symbol	Meaning
31:21	RESERVED	Reserved for future use.
20:0	CSIZE[20:0]	This field reflects the value of the size (bytes) of the current DMA transaction.

4.2.4.5 VID_CCNT Register

This register is used to view the (byte) count of the curently executing DMA transfer.

Table 4-33 VID_CCNT Bit Definition

Bits	Symbol	Meaning
31:21	RESERVED	Reserved for future use.
20:0	CCNT[20:0]	This field reflects the value of the index count of the current DMA transaction. Software can determine how far along the DMA transfer is by reading this register.

4.2.4.6 VID_NSTART Register

This register is used to read and write the starting word address of the next DMA transfer.

Table 4-34 VID_NSTART Bit Definition

Bits	Symbol	Meaning
30:25	RESERVED	Reserved for future use.
26:0	NADDR[26:0]	This field reflects the value of the starting address of the next DMA transaction. IF NADDR[26] = '1', ROM space is accesses as opposed to main memory.

4.2.4.7 VID_NSIZE Register

This register is used to read and write the byte size of the next DMA transfer.

Table 4-35 VID_NSIZE Bit Definition

Bits	Symbol	Meaning
31:21	RESERVED	Reserved for future use.
20:0	NSIZE[20:0]	This field reflects the value of the size (in bytes) of the next DMA transaction. Note that the minimum video transfer is 16 words (64B).

4.2.4.8 VID_DMACNTL Register

This register is used to control the video DMA channel.